## Title: TWO-WIRE INTERFACE HAVING DYNAMICALLY ADJUSTABLE DATA FIELDS DEPENDING ON OPERATION CODE

Inventors: Gerald L. Dybsetter and Jayne C. Hahin Docket No.: 15436.334.1

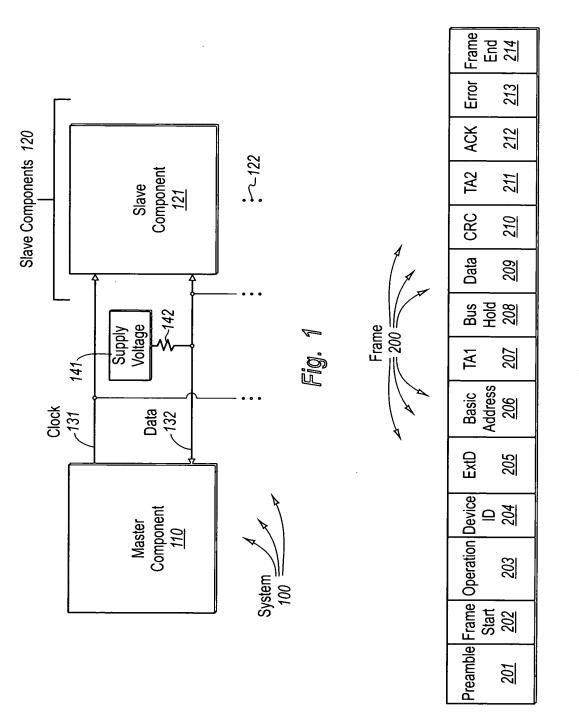


Fig. 2

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DATA FIELDS DEPENDING ON OPERATION CODE Inventors: Gerald L. Dybsetter and Jayne C. Hahin Docket No.: 15436.334.1

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L	/	/	

		<b>Z</b> / <b>I</b>		
Z1 Z2 BT2 Z3 DATA_L CRC ACK E 4 3 2 5 4 3 6 5 4 3 2	Z B DDDDDDDD 0 DDDDDDDD 0 CCCCCCC 0 1 0 0 12 - 301A : ******* * ******* * ******* * * * * *	1 DDDDDDDD 0 DDDDDDDD 0 CCCCCCC Z 1 0 0 1Z	******** * ******* * ******* * * ******	Fig. 3A
ADDR 20 20 3 2 1 4 4 3	; <del></del> 1 * · · ;	* · · · · · · · · · · · · · · · · · · ·	crc_gen: *** *** ***** . ******* . crc_chk: *** *** ****** . ********	

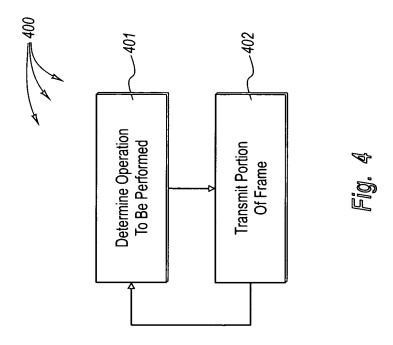
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	12 ~~301C *:	112 ~~304C *.		
BT1 DATA_H Z1 Z2 2 2 1 1 1 1 0 0 0 00 1 0 9 2 1 0 3 2 10		17:		
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128	· N · ·	10* • 1	ત્વ	3
DR	AAAAAAA Z B DDDDDDDD 0 DDDDDDDD 0 ********	AAAAAAA ******************************	(restart if input not all 1's)	Fig. 3C
>m0		1>* 1	· <b>=</b>	
38 Z	·	> * ·	jĖ	
OP DEV 33 3 3 3 3 2 76 5 3 2 0 9	110	010 * * *	art	
SR 33 76	0 * :	10*: 1	est	
Ξ m∞	ı <del>⊢</del> 1∗ •	I <del></del>	ت	
ოი	표 : :	<del> </del>   : :	<del> †</del>	
PRE 3	I : : :	1 :: : !		
	••••	R: H soe:	<b>\ —</b> +	
	RD: moe soe	WR: HH moe: soe:		

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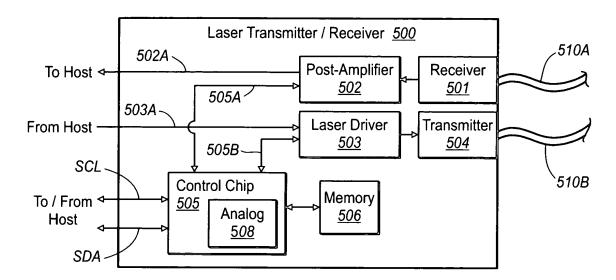


Fig. 5

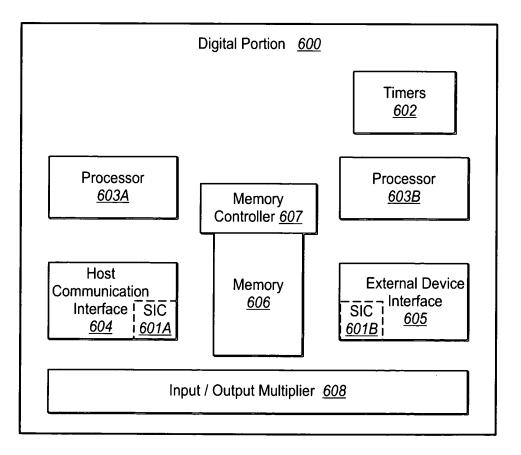


Fig. 6

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		wledge
IDLE 0 0	1 2 2 2 2 1	r ackno
ATA 0 1	AAAAAAA ODDDDDDD ODDDDDDD ODDDDDDD	transfe
ADDRESS/DATA 1 6		preamble start of frame operation code NC=10) port address device address bus turnaround phase & transfer acknowledge address or data end of transmission transaction bit length
TA 11 87	10 10 20 20	ram cod ss iss ires oun da nsm
DEV 2 1 3 9	2 2 2 2     3 2 2 2     3 2 2 2     3 2 2 2	preamble start of frame operation code RDINC=10) port address device address address or data end of transmission transaction bit len
PRT 2 2 8 4	dddd   ddddd   ddddd   dddddd   dddddd	pres star oper RDINC=1 port devi addr end end
0P 32 09	00 01 10 10	
ST 33 21	100001	(32) (2) (2) (2) (5) (5) (5) (16) (16)
PRE 6 3 4 3	11 11 11 11 Bits	 64:33 32:31 30:29 WR=01, R 28:26 25:19 18:17 16:1
	Address Write Read Read inc.	PRE 64:33 (32) preamb ST 32:31 (2) start OP 30:29 (2) operat (ADDR=00, WR=01, RD=11, RDINC=10) PRTAD 28:26 (5) port a DEVAD 25:19 (5) device TA 18:17 (2) bus tu ADDR/DATA 16:1 (16) address IDLE 0 (1) end of